Johannes Walter

Work Experience

Ettus Research (National Instruments), Santa Clara, California — 05/2015 – Present

FPGA and Software Design Engineer

- Work on an R&D team building the Universal Software Radio Peripheral (USRP), a market-leading Software-Defined Radio (SDR).
- Design Verilog components to interface with high-speed RF transceivers and AXI4 IPs on Xilinx FPGAs.
- Build self-checking testbenches in SystemVerilog with constrained-random stimulus generation and perform coverage closure.
- Write Linux user-mode device drivers in C/C++ and C firmware for a SuperSpeed USB controller.

European Organization for Nuclear Research (CERN), Switzerland — 03/2012 – 04/2015

Digital Design and Verification Engineer

- Worked with the team as external contractor through my own business, Greenshire Systems, since October 2014.
- Improved radiation effect mitigation in the Large Hadron Collider (LHC) power converter control electronics.
- Designed radiation tolerant VHDL components, e.g. FIR filters for $\Delta\Sigma$ ADCs, and collaborated with the PCB design team.
- Performed functional verification with SystemVerilog/UVM/SVA and radiation tests to determine circuit reliability.

Electronics Engineer

- On an engineering team for the MedAustron cancer treatment project which operates an ion beam therapy center.
- Developed an FPGA-based interface PCB to ensure reliable communication over fiber optic links for the regulation loop.
- Wrote software in C/C++ for programming FPGAs remotely over Ethernet and SPI.

DICE (Infineon Technologies), Austria — 04/2011 – 02/2012

Design Verification Engineer

- Created a SystemVerilog verification environment for register models using UVM.
- Assisted the component design team thoroughly verifying their implementations.
- Evaluated an OVM extension for SystemC to provide verification features during concept design.

Projects

ricodebug (Open Source Project) — 10/2010 – 06/2011

- Developed an open source GDB front-end in Python and implemented graphs to visually assist debugging of C/C++ data structures.
- Added SystemC features to provide simulation details for systems engineers and ease debugging of SoC concepts.

Hardware Engineering

Digital Design
VHDL, Verilog, SystemVerilog, SystemC, TLM

Design Verification
UVM, SVA, PSL, Random Stimulus, Coverage Closure

Electronics
Schematics capture and PCB layout with Altium

Software Engineering

Programming
C++, C, Python, Assembly

Scripting
TCL, Matlab, Linux Shell Scripts

Web Development
HTML, CSS, JavaScript

Education

University of Applied Sciences Hagenberg, Austria — 2010 – 2012
Master of Science in Engineering – Embedded Systems Design

University of Applied Sciences Hagenberg, Austria — 2007 – 2010
Bachelor of Science in Engineering – Hardware Software Design

Languages

German (native), English (professional – *U.S. Permanent Resident*), Italian (elementary), French (elementary)

Publications

S. Uznanski, B. Todd, **Walter, J.**, and A. Vilar-Villanueva, "COTS FPGA/SRAM irradiations using a dedicated testing infrastructure for characterization of large component batches," in Mixed Design of Integrated Circuits Systems (MIXDES), 2014 Proceedings of the 21st International Conference, pp. 381–384, June 2014.

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